EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	54	("5,630,110" "6,963,990" "6,295,568" "5,630,148" "5,664,165" "5,754,867" "6,763,478" 2004/0139363 "5,790,877" "6,2117" "1" "5" "5,918,061").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 08:23
L2	10	("5,630,110" "6,963,990" "6,295,568" "5,630,148" "5,664,165" "5,754,867" "6,763,478" "20040139363" "5,790,877" "6,2117" "1" "5" "5,918,061").pn.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/17 09:49
L3	1	l1 and bandwidth	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 09:50
L4	3	("5764968" | "5983297" | "6081863").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/17 08:08
L5	10	("6295568").URPN.	USPAT	OR	ON	2006/07/17 08:21
L6	1	("5778237").PN.	USPAT	OR	ON	2006/07/17 08:22
L7	2797	(clock near3 (frequenc$3 or speed or rate))with bandwidth	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 08:24
L8	51	(clock near3 (frequenc$3 or speed or rate))with (bandwidth near3 (information or characteristic$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 09:50
L9	5	((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4)near3 (clock near3 (frequenc$3 or speed or rate)))with (bandwidth near3 (information or characteristic$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 09:53
L10	12	("6,484222" "6,564,279" "6,134,621" "5,930,496" "6,954813" "6,070,207" "6,185,692" "6,772,263" "5,815,734" "6,714,890" "6,948,020" "6,782,438").pn.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/17 09:49

EAST Search History

L11	0	l10 and ((clock near3 (frequenc$3 or speed or rate))with (bandwidth near3 (information or characteristic$1)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 09:50
L12	5	l10 and bandwidth	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 09:50
L13	6	((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4)near3 (clock near3 (frequenc$3 or speed or rate)))with ((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)) near3 (information or characteristic$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 09:55
L14	9	((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))with ((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)) near3 (information or characteristic$1))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 09:59
L15	0	((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))with ((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1))with ((device or chip or IC)near2 (information or characteristic$1)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:36
L16	14	"5935232".uref.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:31
L17	2	"5935232".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:31

EAST Search History

L18	35	("4096571" | "4339808" | "4682282" | "4953081" | "4972313" | "4974148" | "5146596" | "5245322" | "5265223" | "5274763" | "5274784" | "5278974" | "5345566" | "5392033" | "5396602" | "5404463" | "5463624" | "5467454" | "5471590" | "5524235" | "5526017" | "5533205" | "5535341" | "5546546" | "5572686" | "5574867" | "5583999" | "5606557" | "5627975" | "5627976" | "5682484" | "5710892" | "5748806" | "5754548" | "5754807").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/07/17 10:31
L19	0	((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))with (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:39
L20	26526	"713"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:40
L21	0	l20 and (((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))with (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:40
L22	26445	"710"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 12:52

EAST Search History

L23	0	l22 and (((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))with (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:41
L24	0	l22 and (((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))same (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:41
L25	3	l20 and (((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))same (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 12:53
L26	1	(((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))same (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1))))).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 10:42
L27	112504	"455"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 12:53
L28	99515	"370"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 12:53

EAST Search History

L29	66585	"375"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 12:53
L30	0	l27 and (((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))same (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 12:53
L31	0	l28 and (((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))same (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 12:53
L32	0	l29 and (((determin$5 or select$4 or sett$3 or set or chos$3 or choos$4 or generat$4)near3 (clock near3 (frequenc$3 or speed or rate)))same (((device or chip or IC)near2 (information or characteristic$1))with((bandwidth or (bus adj2 width)or (("32" or "64") adj bit$1)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 12:53

Terms used **barr andrew** Found **1** of **178,880**

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Relevance scale

1 Energy constraints on parameterized models

Andrew Witkin, Kurt Fleischer, Alan Barr

August 1987 **ACM SIGGRAPH Computer Graphics , Proceedings of the 14th annual conference on Computer graphics and interactive techniques SIGGRAPH '87**, Volume 21 Issue 4

Publisher: ACM Press

Full text available: pdf(3.73 MB) Additional Information: full citation, abstract, references, citings, index terms

A simple but general approach to imposing and solving geometric constraints on parameterized models is introduced, applicable to animation as well as model construction. Constraints are expressed as energy functions, and the energy gradient followed through the model's parameter space. Intuitively, energy constraints behave like forces that pull and parametrically deform the parts of the model into place. A wide variety of geometric constraints are amenable to this formulation, and may be used t ...

Results 1 - 1 of 1

Nothing Found

Your search for **+abstract:clock +abstract:speed +abstract:rate +abstract:frequency abstract:bandwidth +author:barr** did not return any results.

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Quick Tips

- Enter your search terms in lower case with a space between the terms.

  ```
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  ```

  You can also enter a full question or concept in plain language.

  ```
  Where are the sales offices?
  ```

- Capitalize proper nouns to search for specific people, places, or products.

  ```
  John Colter, Netscape Navigator
  ```

- Enclose a phrase in double quotes to search for that exact phrase.

  ```
  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

  ```
  museum +art
  ```

- Exclude pages by using a - if a search term must not appear on a page.

  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Nothing Found

Your search for **+abstract:clock +abstract:speed +abstract:rate +abstract:frequency abstract:bandwidth +author:somervill** did not return any results.

You may want to try an Advanced Search for additional options.

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  ```
  museum +art
  ```

- Exclude pages by using a - if a search term must not appear on a page.

  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Nothing Found

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Quick Tips

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  ```

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- Enclose a phrase in double quotes to search for that exact phrase.

  ```
  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

  ```
  museum +art
  ```

- Exclude pages by using a - if a search term must not appear on a page.

  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Terms used **clock speed frequency rate bandwidth** Found **8** of **178,880**

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Relevance scale

1 A 4 Gsamples/S with 2-4 GHz Input Bandwidth SIGE Digitizer for Radio Astronomy Applications

D. Deschans, J-B. Begueret, Y. Deval, C. Scarabello, P. Fouillat, G. Montignac, A. Baudry

September 2002 **Proceedings of the 15th symposium on Integrated circuits and systems design**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract

This paper presents the design details and the measurement results of a high speed A/D converter (ADC or digitizer) developed specifically for radio-astronomy applications. This monolithic digitizer is implemented in a SiGe BiCMOS process for high frequency mixed-signal applications. The principal characteristics of this circuit are a 2 bits resolution with 3 quantization levels (or 1.5 bits), a wide input bandwidth from 2 GHz up to 4 GHz and a sampling rate of 4 Gsamples/s (Gsps). The architect ...

2 Processor frequency setting for energy minimization of streaming multimedia application

Andrea Acquaviva, Luca Benini, Bruno Riccò

April 2001 **Proceedings of the ninth international symposium on Hardware/software codesign**

Publisher: ACM Press

Full text available: pdf(401.70 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we describe a software-controlled approach for adaptively minimizing energy in embedded systems for realtime multimedia processing. Energy is optimized by clock speed setting: the software controller dynamically adjusts processor clock speed to the frame rate requirements of the incoming multimedia stream. The speed-setting policy is based on a system model that correlates clock speed with best-case, average-case and worst-case sustainable frame rate, accounting for data-depend ...

3 Architectures: The SFRA: a corner-turn FPGA architecture

Nicholas Weaver, John Hauser, John Wawrzynek

February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(234.25 KB) Additional Information: full citation, abstract, references, index terms

FPGAs normally operate at whatever clock rate is appropriate for the loaded configuration. When FPGAs are used as computational devices in a larger system, however, it is better to employ fixed-frequency FPGAs operating at a high clock frequency. Such fixed-frequency arrays require pipelined interconnect structures, which are difficult to support in a traditional FPGA architecture. We have developed a novel approach, called a "corner-

turn" interconnect, based on a Manhattan array of logically de ...

Keywords: FPGA CAD, FPGA architecture, FPGA design study, FPGA optimization

4 RF and data communication circuits: High speed differential pulse-width control loop based on frequency-to-voltage converters

Hung Tien Bui, Yvon Savaria

April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**

Publisher: ACM Press

Full text available: pdf(127.43 KB) Additional Information: full citation, abstract, references, index terms

A novel differential pulse-width control loop circuit based on high speed frequency-to-voltage converters is proposed. To demonstrate its functionality, a circuit has been designed and simulated in 0.18mm CMOS technology. Results show that the proposed circuit can correct a clock signal's duty cycle even for frequencies as high as 5 GHz. This design can be used to correct clock signal distortion due to process variations in high speed applications such as half-rate clock and data recovery system ...

Keywords: PWCL, duty cycle, frequency-to-voltage, high-speed

5 VSV: L2-Miss-Driven Variable Supply-Voltage Scaling for Low Power

Hai Li, Chen-Yong Cher, T. N. Vijaykumar, Kaushik Roy

December 2003 **Proceedings of the 36th annual IEEE/ACM International Symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(205.58 KB) Additional Information: full citation, abstract, citings, index terms

Energy-efficient processor design is becoming moreand more important with technology scaling and with highperformance requirements. Supply-voltage scaling is anefficient way to reduce energy by lowering the operatingvoltage and the clock frequency of processorsimultaneously. We propose a variable supply-voltagescaling (VSV) technique based on the following keyobservation: upon an L2 miss, the pipeline performs someindependent computations but almost always ends upstalling and waiting for data, d ...

6 Poster session IV: A fractional delay-locked loop for on chip clock generation applications

P. Torkzadeh, A. Tajalli, M. Atarodi

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(469.69 KB) Additional Information: full citation, abstract, references

A fractional multiplying delay-locked loop (FMDLL) for high speed on-chip clock generation applications is presented. The proposed DLL architecture overcomes some drawbacks of phase-locked loops (PLLs) such as jitter accumulation and stability while maintaining the advantageous of a PLL as a multi-rate fractional frequency multiplier.The output frequency range can be tuned from 1GHz to 2.5GHz with selectable multiplication ratios of $M + 0.05 \times K$ where $1 \leqslant K \leqslant 19$. To ge ...

7 Poster session III: Cluster-based detection of SEU-caused errors in LUTs of SRAM-based FPGAs

E. Syam Sundar Reddy, Vikram Chandrasekhar, M. Sashikanth, V. Kamakoti, N. Vijaykrishnan

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(337.50 KB) Additional Information: full citation, abstract, references

This paper proposes a cluster-based parity-checking technique that can detect 100% of all Single Event Upset (SEU) faults in the LUTs of SRAM-based FPGAs. The paper describes two different Configurable Logic Block (CLB) architectures that could be used to implement the proposed SEU detection technique. Of the two, the first architecture can perform at-speed testing of the LUTs without interrupting the normal functioning of the FPGA. The second one works by switching the CLBs from normal-mode to ...

8 Poster session: A high-speed successive erasure BCH decoder architecture

Thomas Buerner

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

A new high speed architecture for a BCH successive erasure decoder is presented. The Berlekamp-Massey based decoder by Sarwate and Shanbhag is extended to handle successive erasures. The critical path in the calculation submodules is increased from Tadd+Tmult to Tadd+Tmult+Tmux. The proposed architecture is implemented exemplary for a BCH(63,45,7) code with up to two erasures on a XILINX Spartan2E300-7. Thus a clock frequency of 95 MHz is reached using 47% of the available slices instead of 105 ...

Results 1 - 8 of 8

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

1. **Cost reduction in the CCD realization of MVMT functions**
   Abd-El-Barr, M.H.; Vranesic, Z.G.;
   Computers, IEEE Transactions on
   Volume 39, Issue 5, May 1990 Page(s):702 - 706
   Digital Object Identifier 10.1109/12.53584
   AbstractPlus | Full Text: PDF(360 KB) IEEE JNL
   Rights and Permissions

2. **Algorithmic synthesis of MVL functions for CCD implementation**
   Abd-El-Barr, M.H.; Vranesic, Z.G.; Zaky, S.G.;
   Computers, IEEE Transactions on
   Volume 40, Issue 8, Aug. 1991 Page(s):977 - 986
   Digital Object Identifier 10.1109/12.83641
   AbstractPlus | Full Text: PDF(796 KB) IEEE JNL
   Rights and Permissions

3. **CMOS multiple-valued logic design. ii. Function realization**
   Jain, A.K.; Bolton, R.J.; Abd-El-Barr, M.H.;
   Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]
   Volume 40, Issue 8, Aug. 1993 Page(s):515 - 522
   Digital Object Identifier 10.1109/81.242321
   AbstractPlus | Full Text: PDF(532 KB) IEEE JNL
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4. **CMOS multiple-valued logic design. i. Circuit implementation**
   Jain, A.K.; Bolton, R.J.; Abd-El-Barr, M.H.;
   Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]
   Volume 40, Issue 8, Aug. 1993 Page(s):503 - 514
   Digital Object Identifier 10.1109/81.242320
   AbstractPlus | Full Text: PDF(764 KB) IEEE JNL
   Rights and Permissions

5. **Pure phase-encoded MRI and classification of solids**
   Ghosh, P.; Laidlaw, D.H.; Fleischer, K.W.; Barr, A.H.; Jacobs, R.E.;
   Medical Imaging, IEEE Transactions on
   Volume 14, Issue 3, Sept. 1995 Page(s):616 - 620
   Digital Object Identifier 10.1109/42.414627
   AbstractPlus | Full Text: PDF(516 KB) IEEE JNL
   Rights and Permissions

6. **Partial-volume Bayesian classification of material mixtures in MR volume data using voxel histograms**
Laidlaw, D.H.; Fleischer, K.W.; Barr, A.H.;
Medical Imaging, IEEE Transactions on
Volume 17, Issue 1, Feb. 1998 Page(s):74 - 86
Digital Object Identifier 10.1109/42.668696
AbstractPlus | References | Full Text: PDF(392 KB) IEEE JNL
Rights and Permissions

7. **Heart-muscle fiber reconstruction from diffusion tensor MRI**
Zhukov, L.; Barr, A.H.;
Visualization, 2003. VIS 2003. IEEE
19-24 Oct. 2003 Page(s):597 - 602
AbstractPlus | Full Text: PDF(575 KB) IEEE CNF
Rights and Permissions

8. **Oriented tensor reconstruction: tracing neural pathways from diffusion tensor MRI**
Zhukov, L.; Barr, A.H.;
Visualization, 2002. VIS 2002. IEEE
27 Oct.-1 Nov. 2002 Page(s):387 - 394
Digital Object Identifier 10.1109/VISUAL.2002.1183799
AbstractPlus | Full Text: PDF(627 KB) IEEE CNF
Rights and Permissions

9. **Fast extraction of adaptive multiresolution meshes with guaranteed properties from volumetric data**
Gavriliu, M.; Carranza, J.; Breen, D.E.; Barr, A.H.;
Visualization, 2001. VIS '01. Proceedings
21-26 Oct. 2001 Page(s):295 - 565
AbstractPlus | Full Text: PDF(879 KB) IEEE CNF
Rights and Permissions

10. **ALCOVE: design and implementation of an object-centric virtual environment**
Meyer, M.; Barr, A.H.;
Virtual Reality, 1999. Proceedings., IEEE
13-17 March 1999 Page(s):46 - 52
Digital Object Identifier 10.1109/VR.1999.756922
AbstractPlus | Full Text: PDF(208 KB) IEEE CNF
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11. **Teleological computer graphics modeling**
Barr, A.H.;
Computer Vision and Pattern Recognition, 1991. Proceedings CVPR '91., IEEE Computer Society Conference on
3-6 June 1991 Page(s):2
Digital Object Identifier 10.1109/CVPR.1991.139650
AbstractPlus | Full Text: PDF(44 KB) IEEE CNF
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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Display Format: Citation Citation & Abstract

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1. **Complex upset mitigation applied to a Re-configurable embedded processor**
Rezgui, S.; Swift, G.; Somervill, K.; George, J.; Carmichael, C.; Allen, G.;
Nuclear Science, IEEE Transactions on
Volume 52, Issue 6, Part 1, Dec. 2005 Page(s):2468 - 2474
Digital Object Identifier 10.1109/TNS.2005.860743
AbstractPlus | Full Text: PDF(568 KB) IEEE JNL
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